Application No.: 10/064,812 Docket No.: JCLA8774

AMENDMENT

In The Claims:

Please amend claims as follows.

Claim 1. (currently amended) A computer main board on/off testing device, comprising: a command translation unit, coupled to the computer main board through a standard interface for receiving and translating a write-in data from a specified port address and latching up the translated write-in data; and a test procedure control unit, coupled to the command translation unit and the computer main board for issuing test control commands according to a preset testing procedure and reading the latched write-in data inside the command translation unit so that functionality of the computer main board is assessed and results are registered.

Claim 2. (original) The computer main board on/off testing device of claim 1, further comprising a test result display unit for displaying the test results.

Claim 3. (original) The computer main board on/off testing device of claim 1, further comprising a test procedure selection unit coupled to the test procedure control unit for selecting the preset testing procedure loop.

Claim 4. (original) The computer main board on/off testing device of claim 1, wherein the preset testing procedure comprises at least one of the following test procedures: on/off test procedure, reset test procedure, and power management suspend/wake up test procedure.

Claim 5. (original) The computer main board on/off testing device of claim 1, further comprising a write-in data display unit for displaying the write-in data.

Claim 6. (original) The computer main board on/off testing device of claim 1, wherein the test control command comprises at least one of the following commands: power switching command and reset command.

Claim 7. (original) The computer main board on/off testing device of claim 1, wherein a time interval between execution of test control commands is programmable.

Claim 8. (original) The computer main board on/off testing device of claim 1, wherein the test procedure control unit comprises a microprocessor, a latching device and a read-only-memory (ROM) unit.

Claim 9. (currently amended) A computer main board on/off testing system, comprising: a computer main board; and_a computer main board testing device connected to a standard interface on the computer main board, wherein the testing device controls the switching and resetting of the computer main board so that test control commands are sequentially transmitted according to a preset testing procedure.

Claim 10. (original) The computer main board on/off testing system of claim 9, wherein the computer main board testing device further comprises a unit for displaying the test results.

Claim 11. (original) The computer main board on/off testing system of claim 9, wherein the test control command comprises at least one of the following commands: power switching command and a reset command.

Claim 12. (original) The computer main board on/off testing system of claim 9, wherein the preset testing procedure comprises at least one of the following test procedures: switching test procedure, reset test procedure, and power management suspend/wake up test procedure.

Claim 13. (original) The computer main board on/off testing system of claim 9, wherein write-in data from a specified port address is read and translated by the standard interface so that functionality of the computer main board is assessed and test results are registered.

Claim 14. (original) The computer main board on/off testing system of claim 9, wherein the test results comprises an error count.

Claim 15. (currently amended) A computer main board on/off testing method, comprising the steps of:_sequentially issuing test control commands according to a preset testing procedure for controlling the switching and resetting of the computer main board; and_retrieving write-in data from a specified port address; and_translating the write-in data through a standard interface on the computer main board so that functionality of the computer main board is assessed and test results are registered.

Claim 16. (original) The computer main board on/off testing method of claim 15, further comprising the step of displaying the test results.

Claim 17. (original) The computer main board on/off testing method of claim 15, wherein the test control command comprises at least one of the following commands: power switching command and reset command.

Claim 18. (original) The computer main board on/off testing method of claim 15, wherein the preset testing procedure further comprises at least one of the following test procedures: on/off test procedure, reset test procedure and power management suspend/wake up test procedure.

Claim 19. (original) The computer main board on/off testing method of claim 15, wherein a time interval between execution of test control commands is programmable.

Claim 20. (original) The computer main board on/off testing method of claim 15, wherein the computer further comprises a computer main board and a computer main board on/off testing device connected to the computer main board for controlling the switching and resetting of the computer main board through a set of connection lines.